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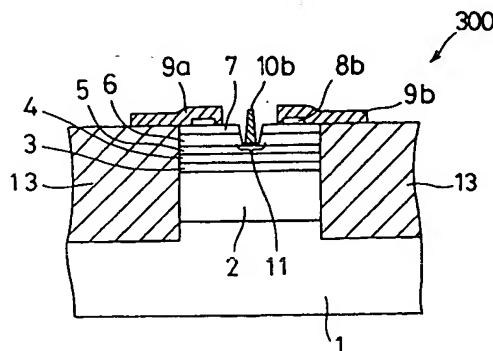
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D-85354 Freising (DE)(54) **Isolated semiconductor device and production method thereof.**

(57) In a method of producing a semiconductor device, when a device, for example, transistor, is formed in a prescribed region of compound semiconductor layers including a low resistance layer which cannot be insulated by ion implantation, upper layers of the compound semiconductor layers including at least the low resistance layer are formed into a mesa shape by etching, and then ion implantation is performed to the compound semiconductor layers in a region other than the region beneath the mesa structure. Thus, the device formed on the substrate is completely isolated from other regions on the substrate by the mesa-etching and the ion implantation. In the structure thus obtained, a level difference on the substrate due to the device is within a range that does not adversely affect the subsequent process steps, for example, a step of producing electrodes. In addition, materials and compositions of the compound semiconductor layers isolated by the mesa-etching are selected according to desired device characteristics without paying considerations on the insulation by ion implantation. Therefore, a degree of freedom in selecting materi-

als and compositions of the compound semiconductor layers formed on the semiconductor substrate increases, resulting in a high-performance device.

Fig. 3

**EP 0 591 607 A2**

FIELD OF THE INVENTION

The present invention relates to a semiconductor device and a production method thereof in which a device is formed in a prescribed region of compound semiconductor layers grown on a semiconductor substrate and, more particularly to a method of isolating the device from other regions on the semiconductor substrate.

BACKGROUND OF THE INVENTION

Figures 5(a) to 5(c) are diagrams illustrating a high electron mobility transistor (hereinafter referred to as HEMT) formed on an InP substrate included in a prior art semiconductor device, in which figure 5(a) is a top plan view and figures 5(b) and 5(c) are sectional views taken along lines Vb-Vb and Vc-Vc of figure 5(a), respectively. In these figures, a mesa structure comprising compound semiconductor layers, i.e., an intrinsic (hereinafter referred to as i type) InAlAs buffer layer 2, an i type InGaAs channel layer 3, an i type InAlAs spacer layer 4, an n type InAlAs electron supply layer 5, an i type InAlAs Schottky formation layer 6, an n type InAlAs layer 7, and a low-resistance n type InGaAs contact layer 8 with carrier concentration of $2 \times 10^{19} \text{ cm}^{-3}$, is disposed on a portion of the InP substrate 1. A recess 11 penetrates through the InGaAs contact layer 8 and the InAlAs layer 7 to reach into the Schottky formation layer 6. A gate electrode 10 is disposed on the Schottky formation layer 6 exposed on the bottom of the recess 11 and extended onto a portion of the substrate 1. Source and drain electrodes 9a and 9b are disposed on the mesa structure where the recess 11 is absent and extended onto portions of the substrate 1. Preferably, the i type InAlAs buffer layer 2 is 1000 ~ 1500 angstroms thick and each of the layers disposed on the buffer layer 2 is 100 ~ 400 angstroms thick. Source and drain regions are formed in the n type InAlAs layer 7. Reference numeral 10a designates a bonding pad at an end of the gate electrode 10, to which wires from external devices or devices disposed on other regions of the InP substrate 1 are bonded.

Figures 6(a) to 6(d) illustrate process steps in a method of producing the HEMT. In the figures, the same reference numerals as in figures 5(a) to 5(c) designate the same or corresponding parts, and reference numeral 12 designates a photoresist pattern.

Initially, there are successively grown on the InP substrate 1, the i type InAlAs buffer layer 2, the i type InGaAs channel layer 3, the i type InAlAs spacer layer 4, the n type InAlAs electron supply layer 5, the i type InAlAs Schottky formation layer 6, the n type InAlAs layer 7, and the n type InGaAs

contact layer 8, preferably by metal organic chemical vapor deposition (MOCVD). Then, a photoresist pattern 12 is formed on the n type InGaAs contact layer 8 by conventional photolithographic technique. Using the photoresist pattern 12 as a mask, the semiconductor layers 2 to 8 are etched by wet etching using tartaric acid or the like as an etchant to form the semiconductor layers 2 to 8 in a mesa shape as shown in figure 6(a). Thus, the mesa-shaped semiconductor layers are isolated from other regions on the InP substrate 1. Then, as shown in figure 6(b), the source and drain electrodes 9a and 9b are formed on prescribed regions on the n type InGaAs contact layer 8, extending onto the surface of the InP substrate 1. Then, recess etching is carried out from the surface of the contact layer 8 while measuring a current flowing between the source and drain electrodes 9a and 9b, whereby the thickness of the i type InAlAs Schottky formation layer 6 in a gate region is adjusted to a desired thickness, resulting the recess 11 shown in figure 6(c). Thereafter, the gate electrode 10 is formed on the i type InAlAs Schottky formation layer 6 exposed on the bottom of the recess 11 by lift-off.

In operation, when a bias voltage is applied between the source and drain electrodes 9a and 9b, a two-dimensional gas serving as a channel is formed in the i type InGaAs channel layer 3 in the vicinity of its boundary with the i type InAlAs spacer layer 4, and a current flows through the channel. This current is controlled by a voltage applied to the gate electrode 10 to operate the transistor.

In a semiconductor device produced by successively growing compound semiconductor layers on a semiconductor substrate and forming a device in a prescribed region of the compound semiconductor layers, like the above-described semiconductor device in which the HEMT is formed on the InP substrate, the thickness of the whole compound semiconductor layers must be larger than 0.2 micron. In addition, in a field effect transistor having a recessed gate, like the above-described HEMT, the thickness of semiconductor layers between the bottom of the recess, on which the gate electrode is formed, and the surface of the semiconductor substrate must be larger than 0.2 micron.

Therefore, in a structure as shown in figure 5(b), in which compound semiconductor layers on a semiconductor substrate are formed in a mesa by etching to isolate a device from other regions on the substrate, a difference in levels between the surface of the semiconductor substrate and the top of the mesa is more than 0.2 micron. In figure 5(b), since the HEMT includes the recessed gate, a difference in levels between the surface of the semiconductor substrate and the bottom of the

recess is more than 0.2 micron. In this structure, when an electrode is formed on the surface of the mesa or on the bottom of the recess extending onto the surface of the substrate, lift-off is usually employed as described above. More specifically, a photoresist film is formed on the mesa and its periphery, and a prescribed portion of the photoresist film is opened by photolithographic technique to form a mask pattern. Then, a metal for the electrode is deposited via the mask pattern, followed by removal of the mask pattern, resulting in an electrode.

In forming a photoresist pattern by the above-described photolithographic technique, a reduced projecting exposure apparatus is generally used for exposure process thereof, and a resolution limit R of the reduced projection exposure apparatus is represented as follows:

$$R = k_1 \lambda / NA \quad (1)$$

where NA is a numerical aperture of a projection lens, λ is a wavelength of exposure light, and k_1 is a constant indicating a lens performance, which is 0.612 in a case of a spherical projection lens according to a theory by Rayleigh. It is known that it is possible to form a fine exposure pattern by increasing the numerical aperture (NA), according to the equation (1).

In forming a photoresist pattern on a substrate having a level difference of 0.2 micron or more, however, a depth of focus is reduced with an increase in the numerical aperture (NA), resulting in an insufficient exposure strength. This makes it very difficult to project a fine exposure pattern having constant light intensity on the substrate having a level difference of 0.2 micron or more. Therefore, in forming a photoresist pattern having an opening of 0.25 micron or below in width is formed, a uniform width of the opening pattern is not obtained and the width also varies in a depth direction of the opening pattern. In this way, in forming the gate electrode 10 on the bottom surface of the recess 11 extending onto the surface of the InP substrate 1 by lift-off in the formation of the HEMT, if the opening of the photoresist pattern is fine-patterned in accordance with a desired width of the gate electrode of 0.25 micron or below, the resulting gate electrode is not uniform in its thickness and width and, in some cases, the gate electrode is discontinuous at the edge of the mesa structure, resulting in a HEMT with poor reliability.

It is thought that this problem may be avoided if the device is isolated by implanting ions into regions where the device is not formed until the ions reach the substrate. In the InP system HEMT with the n type InGaAs layer 8 for contacting with electrodes as an uppermost layer, however, since

the n type InGaAs layer is not insulated by ion implantation, the HEMT is not completely. When compositions of the respective compound semiconductor layers are determined so that these layers can be insulated by ion implantation, compositions of the respective layers preferable in view of device characteristics are not obtained.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor device in which a level difference due to a device formed on a substrate is reduced and the device is completely isolated from other regions on the substrate.

Another object of the present invention is to provide a method for producing the semiconductor device.

Other objects and advantages of the present invention will become apparent from the detailed description given hereinafter; it should be understood, however, that the detailed description and specific embodiment are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

According to an aspect of the present invention, in a method of producing a semiconductor device, when a device is formed in a prescribed region of compound semiconductor layers including a low resistance layer which cannot be insulated by ion implantation, upper layers of the compound semiconductor layers including at least the low resistance layer are formed into a mesa shape by etching, and then ion implantation is performed to the compound semiconductor layers other than those beneath the mesa structure, whereby the device is completely isolated from other regions on the semiconductor substrate. Thus, the device formed on the substrate is isolated from other regions on the substrate using the mesa-etching and the ion implantation, so that a level difference on the substrate due to the device is within a range that does not adversely affect the subsequent process steps, for example, a step of producing electrodes. In addition, materials and compositions of the compound semiconductor layers isolated by the mesa-etching are selected according to desired device characteristics, without paying consideration on the insulation by ion implantation.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1(a) to 1(c) are diagrams illustrating a HEMT formed on an InP substrate included in a semiconductor device in accordance with a first

embodiment of the present invention, in which figure 1(a) is a top plan view and figures 1(b) and 1(c) are sectional views taken along lines 1b-1b and 1c-1c of figure 1(a), respectively;

Figures 2(a) to 2(e) are sectional views illustrating process steps in a method of producing the HEMT of figures 1(a) to 1(c);

Figure 3 is a sectional view illustrating a HEMT formed on an InP substrate included in a semiconductor device in accordance with a second embodiment of the present invention;

Figures 4(a) and 4(b) are sectional views illustrating a HEMT formed on an InP substrate included in a semiconductor device in accordance with a third embodiment of the present invention;

Figures 5(a) to 5(c) are diagrams illustrating a HEMT formed on an InP substrate included in a prior art semiconductor device, in which figure 5(a) is a top plan view and figures 5(b) and 5(c) are sectional views taken along lines Vb-Vb and Vc-Vc of figure 5(a), respectively; and

Figures 6(a) to 6(d) are sectional views illustrating process steps in a method of producing the HEMT of figures 5(a) to 5(c).

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figures 1(a) to 1(c) illustrate a HEMT formed on an InP substrate included in a semiconductor device in accordance with a first embodiment of the present invention, in which figure 1(a) is a top plan view and figures 1(b) and 1(c) are sectional views taken along lines 1b-1b and 1c-1c of figure 1(a), respectively. In the figures, successively disposed on an InP substrate 1 are an i type InAlAs buffer layer 2, an i type InGaAs channel layer 3, an i type InAlAs spacer layer 4, an n type InAlAs electron supply layer 5, an i type InAlAs Schottky formation layer 6, an n type InAlAs layer 7, and an n type InGaAs contact layer 8a. Source and drain electrodes 9a and 9b are disposed on the n type InGaAs contact layer 8a and make an ohmic contact with the contact layer 8a. A recess 11 penetrates through the n type InGaAs contact layer 8a and the n type InAlAs layer 7 to reach into the i type InAlAs Schottky formation layer 6. A gate electrode 10b having a width of 0.25 micron or below is disposed on the i type InAlAs Schottky formation layer 6 exposed on the bottom surface of the recess 11. Reference numeral 13 designates an insulating region for isolating the HEMT 100, which is formed by ion implantation. Source and drain regions are formed in the n type InAlAs layer 7. In addition, the i type InAsAs buffer layer 2 is 1000 ~ 1500 angstroms thick, and each of the layers disposed on the buffer layer 2 is 100 ~ 400 angstroms

thick. The resistance of the n type InGaAs contact layer 8a is reduced by increasing carrier concentration thereof to $1 \times 10^{20}/\text{cm}^3$ order, whereby the source and drain electrodes 9a and 9b can favorably make an ohmic contact with the contact layer 8a. The contact layer 8a is patterned so that edges of the contact layer are aligned with edges of the insulating region 13.

A method of manufacturing the HEMT of figures 1(a) to 1(c) is illustrated in figures 2(a) to 2(d).

Initially, as illustrated in figure 2(a), there are successively grown on the InP substrate 1, the i type InAlAs buffer layer 2, the i type InGaAs channel layer 3, the i type InAlAs spacer layer 4, the n type InAlAs electron supply layer 5, the i type InAlAs Schottky formation layer 6, the n type InAlAs layer 7, and the n type InGaAs contact layer 8a. Preferably, these layers are grown by MOCVD. Then, a photoresist pattern 12 is formed on the n type InGaAs contact layer 8a by a conventional photolithographic technique. Then, using the photoresist pattern 12 as a mask, the n type InGaAs contact layer 8a is selectively etched by wet etching using citric acid as an etchant.

Thereafter, an ion implantation is performed using the photoresist pattern 12 as a mask to form the insulating region 13 penetrating through the semiconductor layers 2 to 7 and reaching into the InP substrate 1 as illustrated in figure 2(b). Here, the n type InGaAs layer 8a which is etched by the wet etching is a layer which cannot be insulated by ion implantation because of its high carrier concentration that provides the low resistance of the layer. Preferably, one of hydrogen (H) ion, boron (B) ion, and iron (Fe) ion, or a combination thereof is used as the ion implanted.

After removing the photoresist pattern 12, the source and drain electrodes 9a and 9b comprising Au alloy or Ag alloy that make an ohmic contact with the n type InGaAs contact layer 8a are formed on the contact layer 8a and portions of the insulating region 13 by lift-off, as illustrated in figure 2(c).

Then, a recess etching is carried out from the surface of the contact layer 8a while measuring a current flowing between the source and drain electrodes 9a and 9b, whereby the thickness of the i type InAlAs Schottky formation layer 6 in a gate region is adjusted to a desired thickness, resulting in the recess 11 shown in figure 2(d).

Then, as illustrated in figure 2(e), the gate electrode 10b having a width of 0.25 micron or below is formed on the Schottky formation layer 6 exposed on the bottom of the recess 11 by lift-off. In the formation of the gate electrode 10b, an aperture width of a photoresist pattern used for selectively depositing an electrode metal on the bottom of the recess is 0.25 micron or below. However, during an exposure process for forming

the photoresist pattern, a difference in levels between the surface of the insulating region 13 and the surface of the Schottky formation layer 6 exposed on the bottom of the recess 11 is in a range of 200 ~ 800 angstroms. Therefore, the pattern exposure is carried out without reducing the resolution and the exposure intensity, whereby a photoresist pattern with a uniform aperture width is obtained. As the result, the gate electrode 10b having uniform width and thickness is formed with no discontinuity at the edge of the insulating region 13. At the same time, an electrode leading part 10a serving as a bonding pad is formed at an end of the gate electrode 10b. Then, wires from a device formed on the other region on the InP substrate 1 or from an external device are bonded onto the bonding pad 10a.

In the semiconductor device according to the first embodiment of the present invention, the uppermost layer of the HEMT 100, i.e., the low resistance n type InGaAs contact layer 8a is isolated from other regions of the compound semiconductor layers by etching, and then the respective layers beneath the contact layer 8a are isolated by ion implantation, whereby the HEMT 100 is completely isolated on the InP substrate 1. In addition, when the gate electrode 10 having a width of 0.25 micron or below is formed on the i type InAlAs Schottky formation layer 6 exposed on the bottom surface of the recess 11, extending onto the surface of the insulating region 13 by lift-off, the difference in levels between the bottom of the recess and the surface of the insulating region 13 is within a range of 200 to 800 angstroms, resulting in a high dimensional precision of the aperture of the photoresist pattern for forming the electrode, and an electrode with uniform width and thickness is attained, with the result that characteristics of the HEMT are improved.

While in the first embodiment the i type InAlAs buffer layer 2 is 1000 ~ 1500 angstroms thick, the buffer layer 2 may be thicker than 1500 angstroms because the increase in the thickness of the buffer layer 2 does not affect the difference in levels between the bottom surface of the recess 11 and the surface of the insulating region 13. In this case, crystallinities of the semiconductor crystal layers 3 to 8a grown on the buffer layer 2 are improved, with a result that characteristics of the HEMT are further improved.

Figure 3 is a sectional view illustrating a HEMT formed on an InP substrate included in a semiconductor device in accordance with a second embodiment of the present invention. In figure 3, the same reference numerals as in figures 1(a) to 1(c) designate the same or corresponding parts. In this second embodiment, width of the n type InGaAs contact layer 8b of the HEMT 300 is narrower than

the width of the n type InGaAs contact layer 8a of the HEMT 100 of the first embodiment, the source and drain electrodes 9a and 9b are disposed over the n type InGaAs contact layer 8a, and intervals between the gate electrode 10b and the source and drain electrodes 9a and 9b are wider than those of the HEMT 100 of the first embodiment.

A method of manufacturing the HEMT 300 is identical to that of the previously described first embodiment except that photolithography and etching for reducing the width of the n type InGaAs contact layer 8b are carried out before the formation of the source and drain electrodes 9a and 9b.

According to the second embodiment of the present invention, the same effects as described in the first embodiment are obtained. In addition, since the width of the n type InGaAs contact layer 8b is narrower and the intervals between the gate electrode 10b and the source and drain electrodes 9a and 9b are wider than those of the HEMT 100 of the first embodiment, a gate junction breakdown voltage is increased, with the result that the characteristics of the HEMT are further improved.

Figure 4(a) is a sectional view illustrating a HEMT formed on an InP substrate included in a semiconductor device in accordance with a third embodiment of the present invention, and figure 4-(b) is a sectional view taken along line IVb-IVb of figure 4(a). In these figures, the same reference numerals as in figures 1(a) to 1(c) designate the same or corresponding parts. Reference numeral 13a designates an insulating region formed by ion implantation.

In this structure, the semiconductor layers on the i type InAlAs buffer layer 2 are formed in a mesa shape by etching, and a prescribed region 13a of the buffer layer 2 and the InP substrate 1 is insulated by ion implantation, whereby the HEMT 400 is isolated from other regions on the InP substrate 1. The gate electrode 10b having a width of 0.25 micron or below is disposed on the bottom surface of the recess 11 and extended onto the surface of the insulating region 13a.

In producing the HEMT 400, time for the mesa-etching of the compound semiconductor crystal layers is controlled in the step of figure 6(a) so as to stop the etching on the surface of the i type InAsAs buffer layer 2, and the insulating region 13a is formed by ion implantation. Thereafter, the source and drain electrodes 9a and 9b and the gate electrode 10b are formed to complete the HEMT 400.

According to the third embodiment of the present invention, in the conventional mesa-etching step of figure 6(a), the etching time is controlled so that a level difference on the substrate may not exceed 0.2 micron, differently from the selective etching in the first and second embodiments of the

present invention. Therefore, the HEMT 400 which is completely isolated from other regions on the substrate is achieved in a simple process. In addition, the fine gate electrode 10b achieved in this embodiment has uniform width and continuity at the edge of the mesa structure because the difference in levels between the surface of the insulating region 13a and the bottom surface of the recess 11 is in a range of 400 to 1600 angstroms.

While in the above-described first to third embodiments the ion implantation is performed after the mesa-etching of the compound semiconductor layers, this order may be reversed.

While in the above-described first to third embodiments the HEMT is formed on the InP substrate, the present invention may be applied to other field effect transistors or other devices formed on semiconductor substrates comprising other materials.

As is evident from the foregoing description, according to the present invention, when a device is formed in a prescribed region of compound semiconductor layers including a low resistance layer which cannot be insulated by ion implantation, upper layers of the compound semiconductor layers including at least the low resistance layer are formed into a mesa shape by etching, and ion implantation is carried out into the compound semiconductor layers other than those beneath the mesa structure, whereby the device is completely isolated from other regions on the semiconductor substrate. Therefore, a device structure with a small level difference is attained, resulting in a high-performance device.

In addition, according to the present invention, materials and compositions of the compound semiconductor layers isolated by the mesa-etching are selected according to desired device characteristics without paying considerations on the insulation by ion implantation. Therefore, the degree of freedom in selecting materials and compositions of the compound semiconductor layers formed on the semiconductor substrate increases, resulting in a high-performance device.

Claims

1. A semiconductor device comprising:
 - a semiconductor substrate;
 - compound semiconductor layers disposed on said semiconductor substrate;
 - a device formed in a prescribed region of said compound semiconductor layers:
 - upper layers of said compound semiconductor layers being isolated from other regions on said semiconductor substrate by mesa-etching; and
 - lower layers of said compound semicon-

ductor layers being isolated from other regions on said semiconductor substrate by an insulating region formed around said lower layers by ion implantation.

2. The semiconductor device of claim 1 wherein said upper layers of said compound semiconductor layers include a low resistance layer which cannot be insulated by ion implantation.
3. The semiconductor device of claim 2 wherein a low resistance layer for producing an ohmic contact, which cannot be insulated by ion implantation, is present at the top of the compound semiconductor layers.
4. The semiconductor device of claim 3 wherein said low resistance layer is an n type InGaAs layer.
5. The semiconductor device of claim 1 wherein a difference in levels between a surface on which an electrode of said device is disposed and the surface of said insulating region on which a portion of said electrode is disposed is below 0.2 micron.
6. The semiconductor device of claim 5 wherein said device is a field effect transistor and said electrode is a gate electrode.
7. A method of producing a semiconductor device, comprising:
 - successively growing compound semiconductor layers on a semiconductor substrate;
 - forming a photoresist pattern with a prescribed width on a region of said compound semiconductor layers where a device is to be formed;
 - etching said upper layers of said compound semiconductor layers in a mesa shape using said photoresist pattern as a mask; and
 - insulating a prescribed region of said compound semiconductor layers by ion implantation to isolate the region where the device is to be formed from other regions on the semiconductor substrate.
8. The method of claim 7 wherein upper layers of said semiconductor layers include a low resistance layer that cannot be insulated by ion implantation.
9. The method of claim 8 wherein said low resistance layer that cannot be insulated by ion implantation is a low resistance layer for producing an ohmic contact and disposed at the top of the compound semiconductor layers.

10. The method of claim 7 wherein one of hydrogen ion, boron ion, and iron ion, or a combination thereof is used in said ion implantation.

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11. The method of claim 9 wherein said low resistance layer for ohmic contact is an n type InGaAs layer.

12. The method of claim 7 wherein said compound semiconductor layers are etched in a mesa shape so that a difference in levels between a surface on which an electrode of said device is disposed and a surface of said region insulated by ion implantation may be below 0.2 micron.

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13. The method claim 11 wherein said device is a field effect transistor and said electrode is a gate electrode.

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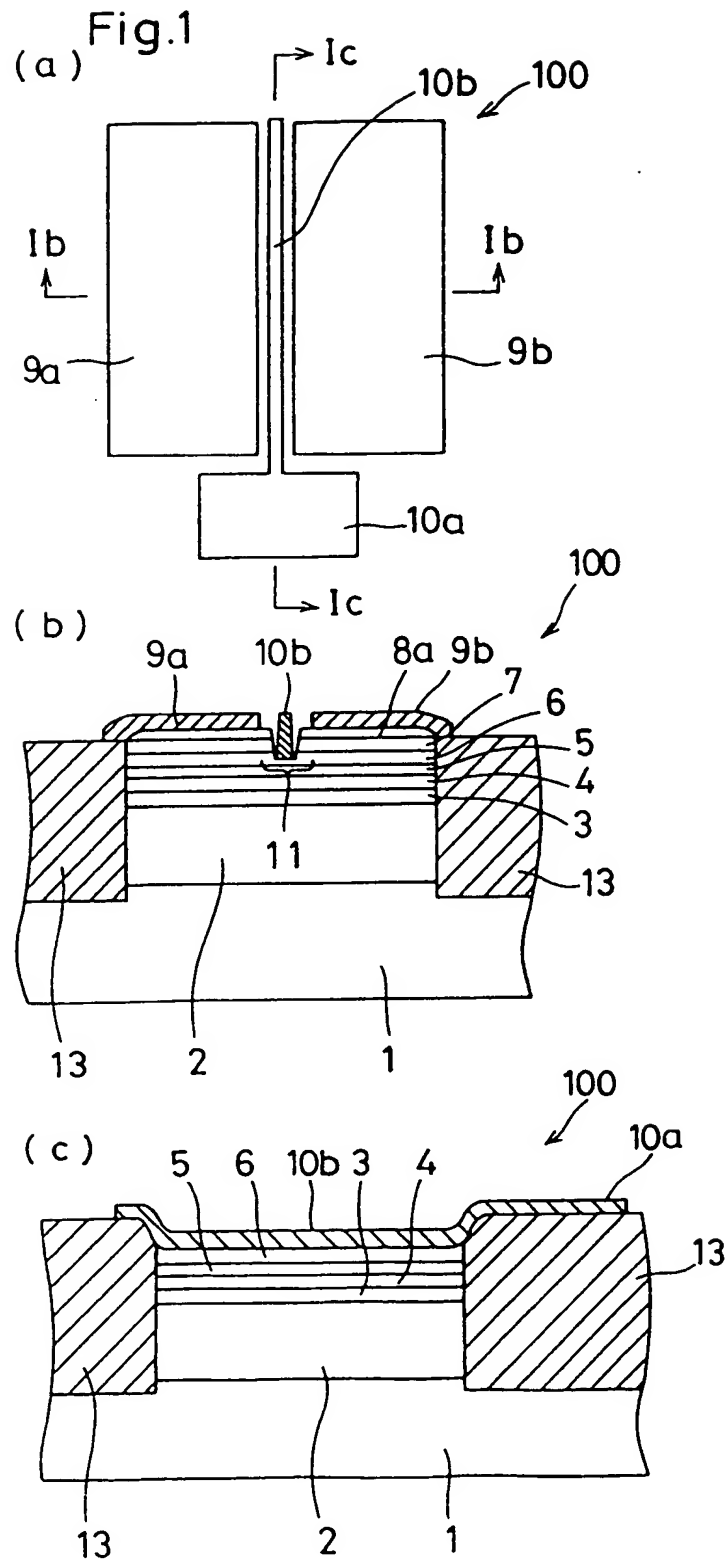
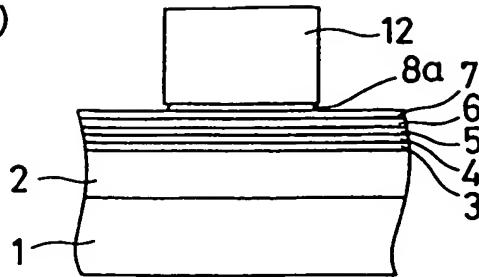
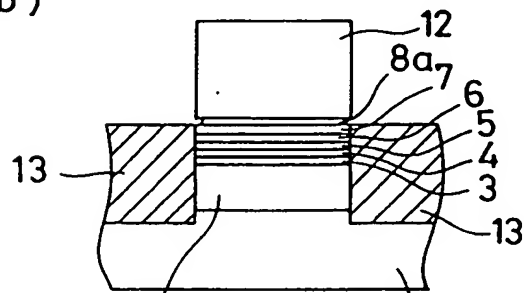


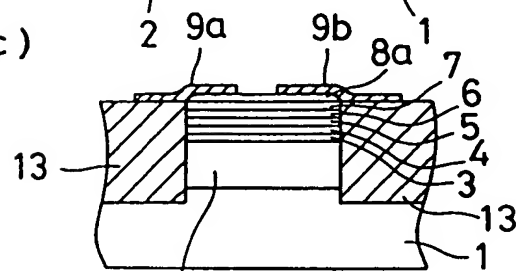
Fig.2
(a)



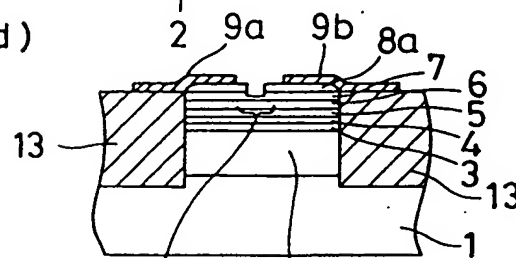
(b)



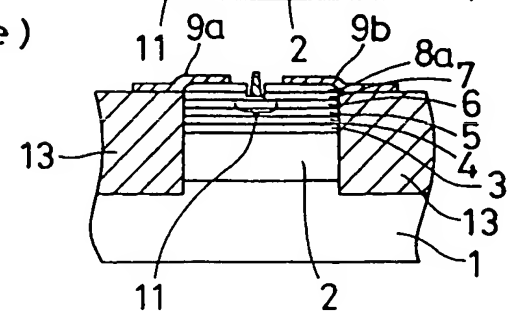
(c)



(d)



(e)

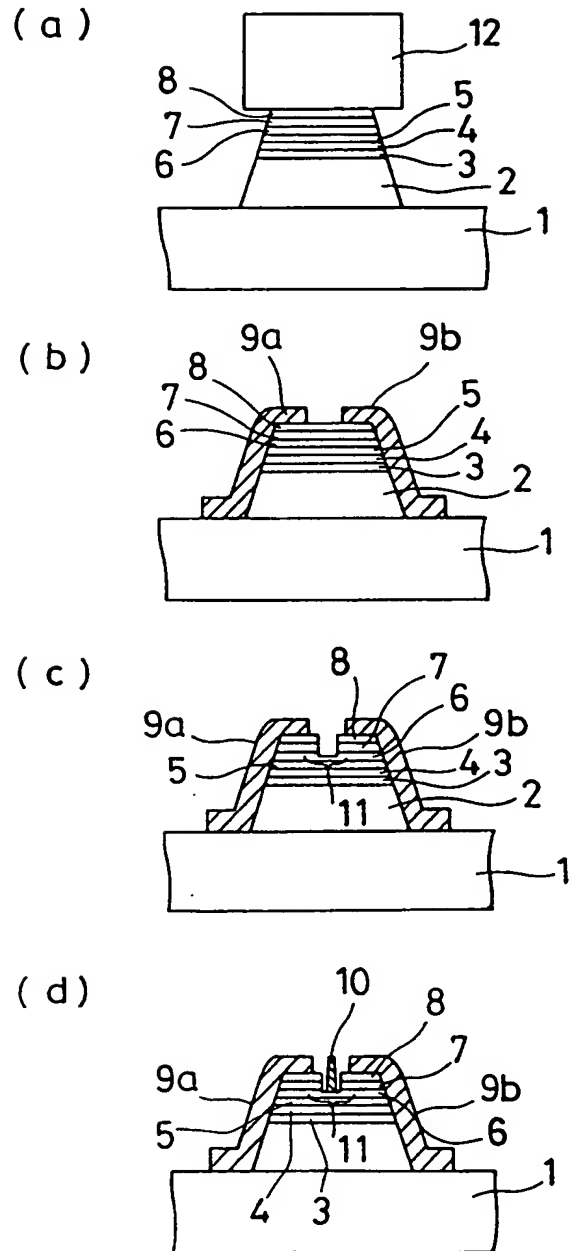


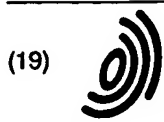
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2.



Fig.6 (Prior Art)





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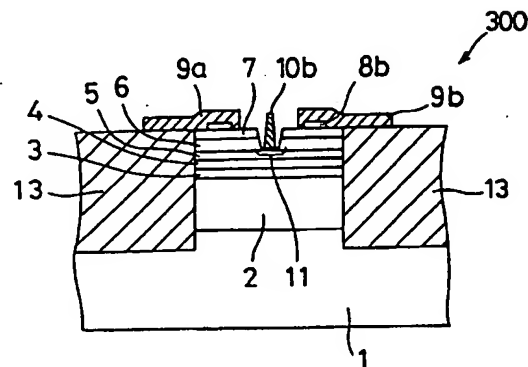
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(54) Isolated semiconductor device and production method thereof

(57) In a method of producing a semiconductor device, when a device, for example, transistor, is formed in a prescribed region of compound semiconductor layers including a low resistance layer which cannot be insulated by ion implantation, upper layers of the compound semiconductor layers including at least the low resistance layer are formed into a mesa shape by etching, and then ion implantation is performed to the compound semiconductor layers in a region other than the region beneath the mesa structure. Thus, the device formed on the substrate is completely isolated from other regions on the substrate by the mesa-etching and the ion implantation. In the structure thus obtained, a level difference on the substrate due to the device is within a range that does not adversely affect the subsequent process steps, for example, a step of producing electrodes. In addition, materials and compositions of the compound semiconductor layers isolated by the mesa-etching are selected according to desired device characteristics without paying considerations on the insulation by ion implantation. Therefore, a degree of freedom in selecting materials and compositions of the compound semiconductor layers formed on the semiconductor substrate increases, resulting in a high-performance device.

Fig. 3



EP 0 591 607 A3



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 93 10 4466

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	PATENT ABSTRACTS OF JAPAN vol. 016, no. 385 (E-1249), 17 August 1992 & JP-A-04 125940 (NEC CORP), 27 April 1992, * abstract; figure 4 *	1-3, 5-10,12, 13	H01L21/76 H01L29/76 H01L21/335
X	PATENT ABSTRACTS OF JAPAN vol. 014, no. 065 (E-0884), 6 February 1990 & JP-A-01 283943 (HITACHI LTD), 15 November 1989, * abstract; figures 1,2 * * page 255, right-hand column *	1-4,7,8, 10	
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The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 6 November 1996	Examiner Gélébart, J
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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